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EXAMINER	
ROJAS, DANIEL E	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/685,418	KURTS ET AL.
	Examiner	Art Unit
	DANIEL ROJAS	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 October 2010_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1,3-26,34,36,65 and 66_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1,3-26,34,36,65 and 66_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _9/10/10 and 12/29/10_.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3-26, 34, 36, 65 and 66 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 7 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Mamoru (Japanese Publication No 02-274121), hereinafter referred to as Mamoru.

4. For claim 1, Mamoru teaches a programmable delay cell (Figure 1) comprising: a first capacitor coupled to a low supply rail (8); a conductor coupled to an output of said programmable delay cell (wire between the output of 2 and the input of 3); and three or more pass gates coupled in parallel to each other (4_1-4_N), wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the same first capacitor (as shown), wherein impedance of each of said pass gates is to be controlled by an independent control signal (as explained below), such that combined impedance of said pass gates is controlled by at least three control signals. The English abstract states that "the number of closed transfer gates 4_1-4_N is controlled to adjust the delay time in a

more minute step.” This function requires that each transfer gate be controlled by an independent control signal.

5. For claim 7, Mamoru teaches a controller (Figure 1) comprising: an output buffer (9) to generate an electrical signal on a conductor coupled to said controller (output of 9); and a programmable delay cell (2, 4, 8) coupled to said output buffer, wherein said programmable delay cell includes at least: a first capacitor (8) coupled to a low supply rail (as shown); a conductor coupled to an output of said programmable delay cell (output of 2); and three or more pass gates coupled in parallel to each other (4_1-4_N), wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the same first capacitor (as shown), wherein impedance of each of said pass gates is to be controlled by an independent control signal, such that combined impedance of said pass gates is controlled by at least three control signals (as explained below). The English abstract states that "the number of closed transfer gates 4_1-4_N is controlled to adjust the delay time in a more minute step.” This function requires that each transfer gate be controlled by an independent control signal.

6. For claim 18, Mamoru teaches a controller comprising: an input buffer (2) to receive an electrical signal from a conductor coupled to said controller (via T1); and a programmable delay cell (4, 8) coupled to said input buffer, wherein said programmable delay cell includes at least: a first capacitor (8) coupled to a low supply rail (as shown); a conductor coupled to an output of said programmable delay cell (conductor to which node N is coupled to); and three or more pass gates coupled in parallel to each other

(4_1-4_N), wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the same first capacitor (as shown), wherein impedance of each of said pass gates is to be controlled by an independent control signal, such that combined impedance of said pass gates is controlled by at least three control signals (as explained below). The English abstract states that "the number of closed transfer gates 4_1-4_N is controlled to adjust the delay time in a more minute step." This function requires that each transfer gate be controlled by an independent control signal.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 3-6, 8-17, 19-26, 34, 36, 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mamoru.

10. For claim 3, examiner takes official notice that an inverter is commonly implemented in a push-pull configuration comprising a pullup PMOS transistor receiving the input signal at its gate and having its drain terminal connected to the output node and a pulldown NMOS transistor receiving the input signal at its gate and having a drain terminal connected to the output node. It would have been obvious to implement Mamoru's inverter 2 in a push-pull configuration as described above since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. Thus, the modified version of Mamoru further teaches a variable impedance transistor (the said PMOS) coupled to a high supply rail and to said conductor, wherein an impedance of said variable impedance transistor is to be determined by a control signal (T1, as explained below). Based on a signal applied to the gate, the transistors will turn on or off. The impedance of the output signal for each transistor is determined by the signal applied to its gate. Thus, the transistors have a variable impedance since they both have two states (a high impedance state and a low impedance state).

11. For claim 4, Mamoru fails to teach a variable impedance transistor. However, examiner takes official notice that it is notoriously old and well known in the art that inverters can be implemented such that they are controlled by both an input signal and an enable signal, wherein 2 PMOS transistors are in series between the positive power supply and the output node and 2 NMOS transistors are in series between the output

node and ground, the gate of the upper PMOS transistor is coupled to an enable signal and the gate of the lower NMOS transistor is coupled to an inverted enable signal. Therefore, it would have been obvious to one of ordinary skill in the art to implement Mamoru's inverter 2 using the implementation as defined above in order to reduce power (by disabling the circuit when not in use). Furthermore, all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. Thus, the modified version of Mamoru as defined above teaches a programmable delay cell (Figure 1) comprising: a conductor (wire between the output of 2 and the input of 3) coupled to an output of said programmable delay cell (as shown); a switch transistor (middle PMOS receiving T_1) coupled to the conductor; three or more pass gates (4_1-4_N) coupled in parallel to each other (as shown), wherein a first terminal of each of the three or more pass gates is coupled to the conductor (as shown) and a second terminal of the each of the three or more pass gates is coupled to one same capacitor coupled to a low supply rail (as shown); and a variable impedance transistor (upper PMOS receiving the enable signal) coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch transistor and the variable impedance transistor (as shown), wherein an impedance of said variable impedance transistor is to be determined by a control signal (inherent based upon the structure).

12. For claim 5, the limitations related only to the intended use of the control signal. It is noted that the circuit which generates the control signal is not being claimed. Note MPEP section 2114 which indicates that "the manner of operating a device does not differentiate an apparatus claim from the prior art" (emphasis added). Applicant should also note the holdings in In re Masham, 2 USPQ2d 1647 (1987); In re Schreiber, 44 USPQ2d 1429 (1997); In re Swinehart, 169 USPQ 226 (1971); In re Casey, 152 USPQ 235 (1967); In re Danly, 120 USPQ 528 (1959); and Hewlewtt-Packard Co. v. Bausch & Lomb, 15 USPQ 1525 (1990). Each of these cases has held that apparatus claims must be structurally distinguishable from the apparatus of the prior art to be patentable, and that the claimed manner in which the apparatus is intended to be used or operated cannot be relied upon for patentability. Moreover, it has been long held that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to those things to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on, see In re Swinehart, 58 CCPA 1027, 169 USPQ 226 (1971).

13. For claim 6, the modified version of Mamoru further teaches that said control signal is a continuous signal (an enable signal is inherently a continuous signal).

14. For claim 8, examiner takes official notice that a variable delay circuit is commonly used in delay locked loops. Therefore, it would have been obvious to use Mamoru's variable delay circuit within a delay locked loop since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. It is known that delay circuits use shift registers to control the plurality of control signals which set the delay value of the variable delay line. Thus, the combination as defined above teaches a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

15. For claim 9, examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

16. For claim 10, the implementation of the controller defined by claim 7 as a memory controller does not further define the structure of the controller. Therefore, the use of the controller as defined by claim 7 as a memory controller relates only to the

intended use of claim 7. Furthermore, the combination circuit of Mamoru teaches a controller which is capable of being a memory controller.

17. For claim 11, Mamoru fails to teach one or two registers coupled to said output buffer. However, Ota teaches in his Figure 14 a programmable output buffer comprising one or two registers (within 304, as explained below) coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer (as explained below). Ota teaches that “the control circuit 304 comprises an n bit shift register, which is shifted up by a pulse of signal 216 and is shifted down by a pulse of signal 217. The content of the register is outputted as signals 229. According to a state of n bit signals 229 which is outputted from the control circuit 304, each tri-state buffer TS1-TSn are switched to an active or a disable state. The current which is supplied to the load is increased by increasing the number of tri-state buffers which are turned active.” It would have been obvious to one of ordinary skill in the art to use Ota's programmable output buffer in place of Mamoru’s output buffer 9 in order to provide a means of regulating driving current. Furthermore, the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

18. For claim 12, Mamoru teaches a controller (Figure 1) comprising: an output buffer (9) to generate an electrical signal on a conductor coupled to said controller (output of 9); and a programmable delay cell (2, 4, 8) coupled to said output buffer, wherein said programmable delay cell includes at least: a first capacitor (8) coupled to a

low supply rail (as shown); a conductor coupled to an output of said programmable delay cell (output of 2); and three or more pass gates coupled in parallel to each other (4_1-4_N), wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the conductor and a second terminal of each of the three or more pass gates is coupled to one same first capacitor coupled to a low supply rail (as shown) but fails to teach a switch transistor or a variable impedance transistor. However, examiner takes official notice that it is notoriously old and well known in the art that inverters can be implemented such that they are controlled by both an input signal and an enable signal, wherein 2 PMOS transistors are in series between the positive power supply and the output node and 2 NMOS transistors are in series between the output node and ground, the gate of the upper PMOS transistor is coupled to an enable signal and the gate of the lower NMOS transistor is coupled to an inverted enable signal. Therefore, it would have been obvious to one of ordinary skill in the art to implement Mamoru's inverter 2 using the implementation as defined above in order to reduce power (by disabling the circuit when not in use). Furthermore, all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. Thus, the modified version of Mamoru as defined above teaches a switch transistor (middle PMOS receiving T_1) coupled to the conductor and a variable impedance transistor (upper PMOS receiving the enable signal) coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch transistor and the variable impedance transistor (as shown), wherein an impedance of said variable impedance transistor is to be determined by a control signal (inherent based upon the structure).

19. For claim 13, the limitations related only to the intended use of the control signal. It is noted that the circuit which generates the control signal is not being claimed. Note MPEP section 2114 which indicates that "the manner of operating a device does not differentiate an apparatus claim from the prior art" (emphasis added). Applicant should also note the holdings in In re Masham, 2 USPQ2d 1647 (1987); In re Schreiber, 44 USPQ2d 1429 (1997); In re Swinehart, 169 USPQ 226 (1971); In re Casey, 152 USPQ 235 (1967); In re Danly, 120 USPQ 528 (1959); and Hewlewtt-Packard Co. v. Bausch & Lomb, 15 USPQ 1525 (1990). Each of these cases has held that apparatus claims must be structurally distinguishable from the apparatus of the prior art to be patentable, and that the claimed manner in which the apparatus is intended to be used or operated cannot be relied upon for patentability. Moreover, it has been long held that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to those things to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does

not possess the characteristic relied on, see In re Swinehart, 58 CCPA 1027, 169 USPQ 226 (1971).

20. For claim 14, examiner takes official notice that a variable delay circuit is commonly used in delay locked loops. Therefore, it would have been obvious to use Mamoru's variable delay circuit within a delay locked loop since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. It is known that delay circuits use shift registers to control the plurality of control signals which set the delay value of the variable delay line. Thus, the combination as defined above teaches a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

21. For claim 15, examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

22. For claim 16, the implementation of the controller defined by claim 7 as a memory controller does not further define the structure of the controller. Therefore, the

use of the controller as defined by claim 7 as a memory controller relates only to the intended use of claim 7. Furthermore, the combination circuit of Mamoru teaches a controller which is capable of being a memory controller.

23. For claim 17, Mamoru fails to teach one or two registers coupled to said output buffer. However, Ota teaches in his Figure 14 a programmable output buffer comprising one or two registers (within 304, as explained below) coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer (as explained below). Ota teaches that “the control circuit 304 comprises an n bit shift register, which is shifted up by a pulse of signal 216 and is shifted down by a pulse of signal 217. The content of the register is outputted as signals 229. According to a state of n bit signals 229 which is outputted from the control circuit 304, each tri-state buffer TS1-TSn are switched to an active or a disable state. The current which is supplied to the load is increased by increasing the number of tri-state buffers which are turned active.” It would have been obvious to one of ordinary skill in the art to use Ota's programmable output buffer in place of Mamoru’s output buffer 9 in order to provide a means of regulating driving current. Furthermore, the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

24. For claim 19, examiner takes official notice that a variable delay circuit is commonly used in delay locked loops. Therefore, it would have been obvious to use Mamoru's variable delay circuit within a delay locked loop since all the claimed elements

were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. It is known that delay circuits use shift registers to control the plurality of control signals which set the delay value of the variable delay line. Thus, the combination as defined above teaches a register coupled to said programmable delay cell to store a value

25. For claim 20, examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

26. For claim 21, the implementation of the controller defined by claim 7 as a memory controller does not further define the structure of the controller. Therefore, the use of the controller as defined by claim 7 as a memory controller relates only to the intended use of claim 7. Furthermore, the combination circuit of Mamoru teaches a controller which is capable of being a memory controller.

27. For claim 22, Mamoru teaches a controller comprising: an input buffer (2) to receive an electrical signal from a conductor coupled to said controller (via T1); and a programmable delay cell (4, 8) coupled to said input buffer, wherein said programmable

delay cell includes at least: a first capacitor (8) coupled to a low supply rail (as shown); a conductor coupled to an output of said programmable delay cell (output of 2); and three or more pass gates coupled in parallel to each other (4_1-4_N), wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the conductor and a second terminal of each of the three or more pass gates is coupled to one same first capacitor coupled to a low supply rail (as shown) but fails to teach a switch transistor or a variable impedance transistor. However, examiner takes official notice that it is notoriously old and well known in the art that inverters can be implemented such that they are controlled by both an input signal and an enable signal, wherein 2 PMOS transistors are in series between the positive power supply and the output node and 2 NMOS transistors are in series between the output node and ground, the gate of the upper PMOS transistor is coupled to an enable signal and the gate of the lower NMOS transistor is coupled to an inverted enable signal. Therefore, it would have been obvious to one of ordinary skill in the art to implement Mamoru's inverter 2 using the implementation as defined above in order to reduce power (by disabling the circuit when not in use). Furthermore, all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. Thus, the modified version of Mamoru as defined above teaches a switch transistor (middle PMOS receiving T_1) coupled to the conductor and a variable impedance transistor (upper PMOS receiving the enable signal) coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch transistor and the variable impedance transistor (as shown), wherein an impedance of said variable impedance transistor is to be determined by a control signal (inherent based upon the structure).

28. For claim 23, the circuit which generates the control signal is not comprised in the apparatus of claim 22. Therefore, the use of a particular control signal relates only to the intended use of claim 22. Furthermore, Mamoru's control signal is capable of being responsive to changes resulting, at least in part, from variations in a supply voltage to said controller, variations in an ambient temperature and variations in a temperature of said controller.

29. For claim 24, examiner takes official notice that a variable delay circuit is commonly used in delay locked loops. Therefore, it would have been obvious to use Mamoru's variable delay circuit within a delay locked loop since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. It is known that delay circuits use shift registers to control the plurality of control signals which set the delay value of the variable delay line. Thus, the combination as defined above teaches a register coupled to said programmable delay cell to store a value

30. For claim 25, examiner takes official notice that it is notoriously old and well known that registers can be initialized by a memory device and/or receive data from a lookup table within a memory device. Therefore, it would have been obvious to one of ordinary skill in the art to use a memory device to store one or more values to program said register since the technique for improving a similar class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

31. For claim 26, the implementation of the controller defined by claim 7 as a memory controller does not further define the structure of the controller. Therefore, the use of the controller as defined by claim 7 as a memory controller relates only to the intended use of claim 7. Furthermore, the combination circuit of Mamoru teaches a controller which is capable of being a memory controller.

32. For claim 34, examiner takes official notice that many circuits and chips and be implemented on a circuit board and therefore, any circuit is capable of being implemented on the same printed circuit board as a graphics chip. Mamoru teaches a controller (Figure 1) including at least a programmable delay cell (Figure 1), said programmable delay cell including at least: a first capacitor coupled to a low supply rail (8); a conductor coupled to an output of said programmable delay cell (wire between the output of 2 and the input of 3); and three or more pass gates coupled in parallel to each other (4_1-4_N), wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the same first capacitor (as shown), wherein impedance of each of said pass

gates is to be controlled by an independent control signal (as explained below), such that combined impedance of said pass gates is controlled by at least three control signals. The English abstract states that "the number of closed transfer gates 4_1-4_N is controlled to adjust the delay time in a more minute step." This function requires that each transfer gate be controlled by an independent control signal. Therefore, it would have been obvious to one of ordinary skill in the art to implement Mamoru's circuit on the same printed circuit board as a graphics chip since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention.

33. For claim 36, examiner takes official notice that an inverter is commonly implemented in a push-pull configuration comprising a pullup PMOS transistor receiving the input signal at its gate and having its drain terminal connected to the output node and a pulldown NMOS transistor receiving the input signal at its gate and having a drain terminal connected to the output node. It would have been obvious to implement Mamoru's inverter 2 in a push-pull configuration as described above since all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions and the combination would have yielded predictable results tone of ordinary skill in the art at the time of the invention. Thus, the modified version of Mamoru further teaches a variable impedance transistor (the said PMOS) coupled to a

high supply rail and to said conductor, wherein an impedance of said variable impedance transistor is to be determined by a control signal (T1, as explained below). Based on a signal applied to the gate, the transistors will turn on or off. The impedance of the output signal for each transistor is determined by the signal applied to its gate. Thus, the transistors have a variable impedance since they both have two states (a high impedance state and a low impedance state).

34. For claim 65, Mamoru further teaches that the second terminal of the each of the three or more pass gates is coupled directly to a node which is then coupled directly to the first capacitor, wherein no other capacitor is disposed between the second terminal and the node, wherein only one capacitor is disposed between the first conductor and the low supply rail (as shown).

35. For claim 66, Mamoru further teaches that the three or more pass gates are in parallel as the first terminal of each of the pass gates is coupled directly to the first conductor, wherein the second terminal of each of the pass gates is coupled directly to a same node without any intermediate component, wherein time delay of an input signal propagated via the programmable delay cell is controlled at least by changing the combined impendence (inherent based upon the structure).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel Rojas/
Examiner, Art Unit 2816
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